Amendments to the Specification:

Please change the title to this application from "A LOW NOISE VERTICAL VARIABLE GATE CONTROL VOLTAGE JFET DEVCIE IN A BICMOS PROCESS AND METHODS TO BUILD THIS DEVICE" to "AN INTEGRATED CIRCUIT DEVICE WITH A VERTICAL JFET."

TI
01/04/06

Please replace paragraph [0028] with the following amended paragraph:

[0028] The doping of the various regions may be by ion-implant technique, diffusion technique, or other techniques known in the art of semiconductor processing. In this embodiment, the NBL 115 is heavily doped, so is the drain region 204. [[Between]] The channel regions 202 are generally doped more lightly than the gate regions. This is to facilitate the modulation of the effective channel width with a gate voltage. In this embodiment, all electrical wirings are disposed near the top surface of the substrate. Not shown in Figure 2 are regions of silicidation, which are commonly employed in the art for reducing the contact resistance between the semiconductor material and the metallic leads 401. Refractory metals such as nickel, titanium and cobalt are commonly employed in the silicidation process. The process of building the n-channel JFET is described in more detail in the following paragraphs with the aid of figures 3–6.